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CPE 301 - 1104, Fall 2016

Homework 2 Part 1

9/14/2016

1. a. address lines: 13 , data lines: 16

b. address lines: 31 , data lines: 8

c. address lines: 24 , data lines: 32

d. address lines: 18 , data lines: 64

2. a. 16K bytes

b. 2G bytes

c. 64M bytes

d. 2M bytes

3. Address: 10 0011 0011 (binary), 233 (hex)

Memory content: 0000 0100 1011 1100 (binary), 04BC (hex)

6. a. 8 chips are required.

b. 18 address lines are needed to access 256K bytes. The 3 most significant bits are

used for chip select. The 15 lines that follow are connected to the address inputs of all

the 32K x 8 chips.

c. 3 lines must be decoded for the chip select inputs. A 3x8 decoder will be used.

7. a. 16 chips are required.

b. 11 address lines are needed to address 2K bytes. The 4 most significant bits are used

for chip select. The 7 lines that follow are connected to the address inputs of all the

128 x 8 chips.

C. 4 lines must be decoded for the chip select inputs. A 4x16 decoder will be used.